REMARKS

A response to the initial Office Action was due November 14, 2002. A Request for a One-Month Extension of Time and the accompanying fee are enclosed. Accordingly, this Response is timely filed.

Reconsideration of this application, as amended, is respectfully requested. By this Amendment, claim 1 is being amended solely to enhance its clarity, and claims 6 and 14 are being amended to correct an obvious typographical error. New claims 28-30 are being added to further define the implantation energy level of the present invention. Claims 1-30 remain in this case.

Original claim 1 was rejected under 35 U.S.C. 102(b) as allegedly anticipated by Sakurai et al. (European Patent Application Publication No. 0 032 022). Original claims 2-27 stand rejected under 35 U.S.C. 103(a) as allegedly obvious over Sakurai et al., further in view of official notice or Nemoto. These rejections are respectfully, but most strenuously, traversed for the reasons presented below.

An important aspect of the present invention, as defined by amended independent claim 1, is the production of a trough in a semiconductor substrate with an ion implementation energy that maintains the original type of doping of a doped inner area on a surface of the substrate. For example, an n-doped trough is produced in a p-doped semiconductor substrate by means of ion implantation through a mask using an energy that assures that a p-doped inner area remains on a surface of the p-doped semiconductor substrate (conversely, a p-doped trough can be produced in an n-doped semiconductor substrate by means of ion implementation through a mask using an energy that assures that an n-doped inner area remains on the surface of the n-doped semiconductor substrate). This feature is not taught by Sakurai.

The introductory part of Sakurai (column 2, line 20-column 4, line 1) makes reference to a prior art method for producing semiconductor components earlier proposed by Sakurai. It should be noted that only the main method steps are described in this introductory part of the patent, making reference to Figures 2-6 of the patent.

In the example presented in this introductory part of the Sakurai patent, a N^+ type buried layer is formed by phosphorous ions implantation in a P type silicon semiconductor substrate 21. According to the Examiner,

Sakurai et al. teaches a method of forming integrated circuit devices such as transistors, diodes and logic gates which includes providing mask 22 onto semiconductor substrate 21 (Page 2, lines 26-30, and Fig. 2), then forming window 23 delimited by peripheral edge (Page 2, lines 31-38, Fig. 3), then performing ion implantation into semiconductor substrate 21 using mask 22 to form n-doped trough 24 with fringe area of trough 24 extending up to semiconductor substrate 21 and with energy that assure n-doped inner area remains on surface of semiconductor substrate 21 (Page 3, lines 1-12, and Fig. 4), and forming additional n-doped areas 27 and 28 in p-doped inner area and in the fringe area of n-doped trough (Page 3, lines 18-29).

However, according to the inventive method of the present invention, as defined by amended claim 1, an implantation energy is employed that will assure that a p-doped inner area remains on a surface of the p-doped semiconductor substrate when an n-doped trough (or buried layer) is formed in the p-doped semiconductor substrate.

In column 4, lines 2-11 of the Sakurai patent, that inventor recognizes that in his earlier disclosed method, illustrated in Figures 2-6 of the patent, it is difficult to form the tapered portion with a desired inclination at the edge of the masking window. To overcome this difficulty, Sakurai presents an improved method of forming a window having an edge which tapers down to the surface of the substrate and the buried layer, as illustrated in Figures 7-13 of this patent.

The subject matter of claim 1 of the present invention differs from the method of Sakurai (which is more fully detailed below) in that the trough is produced by means of ion implantation using an energy that will assure that an upper inner area (reference number 6 of Figures 1a, 1b and 1c of the present application) surrounded by the buried layer (7) and having the same type doping as the original substrate, remains on the surface of the semiconductor substrate, i.e. a p-doped inner area on a p-doped substrate and an n-doped inner area on an n-doped substrate, respectively.

By contrast, Sukarai produces a trough using an energy that will allow the upper inner area to change the doping, i.e. the inner area of a p-doped substrate will become an n-doped inner area or vice versa. On page 7, lines 31 to 35 Sukarai states:

> *Thereafter, phosphorus ions (P^+) are implanted into the silicon substrate 101 using the silicon dioxide layer 104 as a mask. For example the ion implantation conditions are as follows: acceleration energy 400KeV, and dosage 1 x 10^{15} atoms/cm^2. (emphasis added)*

On page 8, lines 16 to 22, Sakurai states:

An active region 101A of the silicon substrate 101 surrounded by the N^+ type buried layer 105 is inverted in an N type region with a surface impurity concentration of about 1 x 10^{17} atoms/cm^3 by such phosphorus ion implantation. Such inversion is effected because the phosphorus ions are normally distributed (Gaussian distribution) in the ion implanted region. (emphasis added)

Due to the change in the donation in the upper inner area, an additional method step is necessary.

Sakurai discloses on page 9, lines 8 to 13:

Then a window is selectively provided on the silicon dioxide film 106 and/or boron ions are implanted using a photoresist layer (not illustrated) formed on the silicon dioxide film 106 as a mask, and thereby a P type base region 107 is formed on the active region 101A. (emphasis added)

According to the present invention, the above additional method step is not necessary since the doping in the inner area does not change.

For a better understanding, applicant is enclosing two figures showing the implantation energy as a function of the depth that are based on measurements of the inventors and computer simulation.

Fig. 1 shows the implantation energy as a function of the depth for an implantation dose of 1e15cm-2. The substrate doping is 1e15cm-3 and 2.5e15cm-3, respectively. It should be noted that the implantation dose of 1e15cm-2 and the substrate doping of 1e15cm-3 are the values as used by Sukarai. As can be seen, if the implantation energy is 6MeV, the doping does not change. By contrast, if the implantation energy is 400KeV as proposed by Sakurai, the doping will change. The upper inner area remaining on the substrate is designated with yellow highlighting. It is not possible to assure that the upper inner layer remains unchanged using an energy of 400KeV as proposed by Sukarai.

Fig. 2 shows the implantation energy as a function of the depth for an implantation dose of 2.5e13cm-2 according to the present invention (6MeV and 2MeV). The substrate doping is 1e15cm-3 and 2.5e15cm-3, respectively.

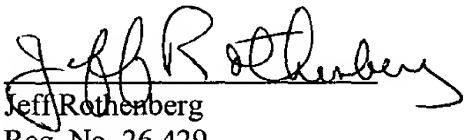
An important aspect of the present invention is the use of a high implantation energy, e.g. 6MeV or 2MeV, so that the doping of the upper inner area does not change and any additional

method step for rechanging of the doping is not necessary. This feature is not taught by Sakurai, nor the secondary reference of Nemato nor common knowledge.

Accordingly, claim 1 and all of the dependent claims that depend therefrom, are believed to be in condition for allowance, and such action is respectfully requested.

Attached hereto is a marked-up version of the changes made to the application by the current amendment. The attachment is entitled "Version with Markings to Show Changes Made."

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method for producing integrable semiconductor components, in particular transistors, diodes, and logic gates, starting with a p-doped or n-doped semiconductor substrate in the following steps:

application of a mask onto the semiconductor substrate for definition of a window delimited by a peripheral edge;

production of an n-doped trough in the p-doped semiconductor substrate or p-doped trough in the n-doped semiconductor substrate by means of ion implantation through the mask using an energy that will assure that a p-doped inner area remains on a surface of the p-doped semiconductor substrate or an n-doped inner area remains on a surface of the n-doped semiconductor substrate, whereby a fringe area of the n-doped trough or p-doped trough extends up to the surface of the semiconductor substrate; and

production of additional n-doped and/or p-doped areas in the p-doped or n-doped inner area and in the fringe area of the n-doped or the p-doped trough that form the structure of the semiconductor component.

6. (Amended) The method of Claim 5, wherein the p-doped area forming the emitter of the transistor has heavier doping [that] than that of the semiconductor substrate.

14. (Amended) The method of Claim 13, wherein a p-doped area having heavier doping [that] than that of the p-doped inner area is inserted in the regions of the p-doped inner area forming the drain and the source, respectively.

28. (New) The method of claim 1 wherein the energy of said ion implantation is at least 2 MeV.

29. (New) The method of claim 1 wherein the energy of said ion implantation is about 6 MeV.

30. (New) The method of claim 1 wherein the ion implantation energy is 6 MeV phosphorous ions at a dose of 2×10^{13} atoms/cm^2.